AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph no. [08] with the following amended paragraph:

According to a first aspect of the present invention, a thin-film semiconductor device comprises a plurality of thin-film transistors (TFTs) having different driving voltages formed on an glass substrate, wherein a gate ~~electrode~~ insulator electric field at each of the driving voltages of the plurality of thin-film transistors is in a range of about 1MV/cm to 2MV/cm, and a drain concentration of p-type thin-film transistors (TFT) is in a range of about $3E+19/cm^3$ to $1E+20/cm^3$. Here the drain concentration means atomic density as well as the carrier concentration for electric conductivity. Ordinarily impurities are doped in a range of atomic density and activated appropriately, such that the atomic density is substantially similar to the carrier concentration. However, even if the atomic density and the carrier concentration are not substantially similar, the range of the atomic density of about $3E+19/cm^3$ to $1E+20/cm^3$ can assist the effect of the present invention.

Please replace the paragraph no. [09] with the following amended paragraph:

Thus, according to the present invention, it is possible to form simply a plurality of thin-film transistors (TFTs) having different driving voltages formed on an glass substrate by setting the range of the gate ~~electrode~~ insulator electric field and drain concentration. The range of the gate ~~electrode~~ insulator electric field may be in the range of 1MV/cm to 2MV/cm, and the range of the drain concentration of the P-type TFTs may be in the range of $3E+19/cm^3$ to $1E+20/cm^3$. In other words, it is possible to provide a plurality of TFTs in a greatly improved throughput, by regulating a gate ~~electrode~~ insulator electric field and a drain concentration of P-type TFTs rather than by changing the gate insulating film for each type of TFTs.

Please replace the paragraph no. [23] with the following amended paragraph:

The glass substrate 100 may be on a transparent insulating substrate made of glass or plastic, a silicon oxide film (SiOx). The undercoat layer 102 is provided to prevent an impurity from being diffused from the glass substrate 100 into an active layer and so it is not necessary to form the undercoat layer if an influence of the impurity is negligible. The thickness of the insulating layer is set in that an electric field of a gate ~~electrode~~ insulator at each of the driving voltages may be in a range of about 1MV/cm to 2MV/cm or any part thereof on the each silicon film 106-109 may be substantially same.

Please replace the paragraph no. [28] with the following amended paragraph:

Next, silicon oxide films are formed as the gate insulating films 114-117 by LPCVD, PCVD, sputtering, etc. In the conventional method, the gate insulating films must be partially formed and etched in a process because the film thicknesses of the gate insulating films need to be altered in accordance with the driving voltages of the TFTs. On the other hand, by the method of the present invention the gate insulating films 114-117 can be formed in the same process because it is possible to regulate the electric field of the gate ~~electrode~~ insulator and the drain concentration of the P-type TFTs (Fig.3(b)).

Please replace the paragraph no. [41] with the following amended paragraph:

The second embodiment is different from the first embodiment in that the electric field of the gate ~~electrode~~ insulator is regulated to a range of 0.2MV/cm to 0.8MV/cm. By reducing the upper limit to 1MV/cm or less, it is possible to manufacture the high-voltage and the low-voltage N-type and P-type transistors by self-alignment with a gate insulating film without providing the region 101 additionally. Such a structure makes it possible to further eliminate a

step required to provide the light-doped region 101, thereby simplifying the manufacturing process further.